Post Graduate Diploma in IC Layout Design

Eligibility:
BE/ B.Tech/ MSc. in Electronics/ Electronics & Telecommunication/ Instrumentation/ Electrical/ Computers/ Information Technology/ MCA/ MCS/ AMIE /AMIETE or equivalent.

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<th>Course No.</th>
<th>Title</th>
<th>Credits</th>
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<td>Semester I (Six Months)</td>
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<td></td>
<td>ELICD-101 Foundation Course in Analog VLSI Design</td>
<td>5 (T) + 5 (P)</td>
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<td>ELICD-102 Foundation Course in Digital VLSI Design</td>
<td>5 (T) + 5 (P)</td>
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<td>ELICD-103 Foundation course in CMOS</td>
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<td>ELICD-104 Foundation course IC Layout Design</td>
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<td>ELICD-105 Foundation course in IPR Management</td>
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<td>Semester II (Four Months)</td>
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<td>ELICD-201 Project</td>
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T- Theory, P- Practicals
ELICD-101: Foundation Course in Analog VLSI Design  

PN Junction, CMOS Transistors, Simple MOS Large Signal Model, Small-signal MOS Model, Analog Subcircuits, MOS Switch, MOS and Bipolar Current Source/Sinks, Current Mirrors, Basic principles of analog IC design -Matching, Process and temperature variations,

Introduction to feedback circuits, Loop gain, Reference circuits and voltage regulators, Current and Voltage References, Bandgap Voltage References, Operational Transconductance Amplifiers, General Design Principles of Op Amps, Op-amp application circuits and op-amp characteristics, Transistor-level view of a two-stage op-amp, Output stages, Device high-frequency small-signal models & capacitances, Simplified BW and high-frequency analysis, BW limitations of basic gain stages: common-source and cascode amplifiers, Slew-rate and BW limitations of op-amps, Frequency-response and stability of feedback circuits, Phase and gain margins, Frequency compensation techniques, Cascode Op Amps,

Digital-Analog & Analog-Digital Converters, Analog and mixed devices and circuits, Analog and mixed circuit design strategies and design optimizations, Circuit simulation tools like Cadence, Mentor Graphics, PSPICE, testing and verification, Analog Circuit Modeling

Reference/Text Books

7. Ron Kielkowski, Inside SPICE, McGraw-Hill
10. Gordon W. Roberts and Adel S. Sedra, SPICE, Oxford University
11. R.v. d Plassche “CMOS Analog to Digital and Digital to Analog Converters” Kluwer International
ELICD-102: Foundation Course in Digital VLSI Design       Credits: 5 (T) + 5 (P)

CMOS inverter, characteristics, shift register, Flipflops, other basic cells, case studies, FPGA Design Flow, ASIC Design Flow, Fault Modeling and Simulation CAD VLSI tools, simulators for logic, timing, circuit, device and process optimization, Xilinx, Cadence, Mentor Graphics simulation tools, Hardware description languages for VLSI design, VHDL and Verilog.

Combinatorial logic circuits and Sequential Circuits, Arithmetic and Logic circuits, Comparison circuits, adder, subtraction, look ahead carry, binary multiplication and division, floating and fixed point arithmetic, ALU design, Finite state machines, Control Unit design

Hierarchical design methods Timing Analysis, Setup, Hold Times, Clock skew, Design Tradeoffs: Designing for speed, power, reliability, testability, Power Analysis, Area and Power Dissipation Estimation, Simultaneously switching outputs, VDD/VSS pairs, Ground Bounce, Latch up, Metastability, Design for Testability, Fault Tolerance, Noise considerations for digital IC’s

Reference/Text Books

1. Rabaey, Chandrakasan, and Nikolic, Digital Integrated Circuits, A Design Perspective
2. Weste and Harris CMOS VLSI Design
4. Uyemura, CMOS Logic Circuit Design,
5. Jaeger, Microelectronic Circuit Design
ELICD-103: Foundation Course in CMOS  

Credits: 5 (T)

Introduction To CMOS Processes: Basic Processing Steps (Doping, Photolithography, Etching, Deposition), PN Junction, MOS Transistors, MOS Device Design Equations, Electrical Interaction Of Layers, NMOS And PMOS Cross Section And Operation, Technology Considerations, Diode, BJT, MOS, Characteristics, models, CMOS Inverter Cross Section, CMOS inverter DC, AC Analysis, Design tradeoffs, Introductions to CAD tools, Hierarchical design of VLSIs, interception levels, behavioral description, RTL, Logic circuit, gate, circuits, device and process. Properties of silicon wafers: Mechanical, Electrical, structural, Si wafer growth techniques.

Epitaxial growth, Oxidation, Diffusion, theory of diffusion, Ion implantation, ion implantation system and principles, Metallization: Deposition techniques, Etching: Etch mechanisms,

The cost-volume trade-off, role of design center and foundry, design methodologies, custom and semicustom designs, standard cell, gate array, FPGA, CPLD and PLDs, FPGA Design Flow, ASIC Design Flow, IC design methodology and terminology, IC Packaging and Bonding techniques, Physics of Power Dissipation in a nanometer CMOS, Design of Low Voltage CMOS Circuits, Low Power SRAM Architectures, Power Estimation/Analysis Techniques, Power Optimization Techniques Adaptive Power Supply Systems, Emerging Technologies,

Reference/Text Books
1. N. H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, Addison-Wesley
ELICD-104: Foundation Course in IC Layout Design  
Credits: 5 (T) + 5 (P)


Introduction to Cadence virtuoso-Basic commands, Bind keys, Layout related functions, Layout vs layout, Layout design & verification-Floor planning- hierarchical design, Power planning, Pin placement, Understanding Design rules, DRC / LVS with ASSURA, Assignments- P - cells creation, Simple inverter, D – flip flop, Custom digital layout, Current mirrors/ buffers/ differential pair, Two stage differential amplifier, High current switches, Resistor/Capacitor dividers, “Layout design & verification of LDO”.

Reference/Text Books
2. Baker, Li Boyce, CMOS Circuit Design , Layout and Simulation
4. M.J.S.Smith, Application Specific Integrated Circuits, Addison-Wesley
5. S. Kang and Yusuf Leblebici,
7. H. E. Weste and David Harris, Principles of CMOS VLSI Design, Addison Wesley
8. Dan Clein, Newnes, CMOS IC Layout,

**ELICD-105: Foundation Course in IPR Management**  
Credits: 5 (T)


IPR Regime, Principles of IP Management, Sectoral IPR Debates on IPR and Development, IPRs and technology transfer, IPRs vis-à-vis access & affordability of medicines, Traditional knowledge, IPR and Benefit sharing, Indigenous knowledge and its appropriation, IPR in Semiconductor IC Layout Design, Concept of Integrated Circuit Layout design, Registration of Integrated Circuit Layout design, Semiconductor Chip Protection Copyrights, design registration, design protection, licensing, IP reuse.

**Reference/Text Books**
1. Deborah E. Bouchoux Intellectual Property for Paralegals Cengage Learning

**ELICD – 201 : Project**

An extensive project involving either Layout design of complete VLSI or an exhaustive analysis of the obtained Layout design from the point of view of IP protection/infringement.